AMENDMENT TO THE CLAIMS

1. (Currently Amended) A method of manufacturing a semiconductor device, the method comprising:

forming a single first dielectric layer overlying a substrate;

forming a first barrier layer, comprising a first dielectric barrier material, on the single first dielectric layer with an interface therebetween,

etching to form a ~~first~~ single opening defined entirely by side surfaces of the first dielectric layer and a bottom;

forming a second barrier layer, comprising a second dielectric barrier material different from the first dielectric barrier material, on an upper surface of the first barrier layer overlying the single first dielectric layer, on the side surfaces of the single first dielectric layer defining the ~~first~~ single opening and on the bottom of the opening;

etching, with selectivity to the first barrier layer, to remove the second barrier layer from, and stopping on, the upper surface of the first barrier layer, and to remove the second barrier layer from the bottom of the ~~first~~ single opening, leaving a portion of the second barrier layer as a liner on the side surfaces of the first dielectric layer defining the ~~first~~ single opening; and

filling the single opening with metal to form a lower metal feature.

2. (Original) The method according to claim 1, wherein the first and second dielectric barrier materials are selected from the group consisting of silicon nitride, silicon oxynitride and silicon carbide.

3. (Original) The method according to claim 2, comprising depositing each of the first and second barrier layers by chemical vapor deposition.

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4. (Original) The method according to claim 3, comprising depositing each of the first and second barrier layers at a thickness of about 50Å to about 500Å.

5. (Currently amended) The method according to claim 1, comprising filling ~~the opening~~ single opening with copper (Cu) or a Cu alloy.

6. (Previously amended) A method of manufacturing a semiconductor device, the method comprising:

forming a first dielectric layer overlying a substrate;

forming a first barrier layer, comprising a first dielectric barrier material, on the first dielectric layer;

etching to form a first opening defined by side surfaces of the first dielectric layer and a bottom;

forming a second barrier layer, comprising a second dielectric barrier material different from the first dielectric barrier material, on an upper surface of the first barrier

layer overlying the first dielectric layer, on the side surfaces of the first dielectric layer defining the first opening and on the bottom of the opening;

etching, with selectivity to the first barrier layer, to remove the second barrier layer from, and stopping on, the upper surface of the first barrier layer, and to remove the second barrier layer from the bottom of the first opening, leaving a portion of the second barrier layer as a liner on the side surfaces of the first dielectric layer defining the first opening;

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filling the opening with metal to form a lower metal feature;

forming a third barrier layer, comprising a third dielectric barrier material different from the first dielectric barrier material, on the first barrier layer and on an upper surface of the lower metal feature;

forming a second dielectric layer on the third barrier layer;

forming a fourth barrier layer, comprising a fourth dielectric barrier material, on the second dielectric layer;

forming a third dielectric layer on the fourth barrier layer;

forming a fifth barrier layer, comprising a fifth dielectric barrier material, on the third dielectric layer;

etching to form a dual damascene opening comprising an upper trench portion defined by side surfaces of the third dielectric layer in communication with a lower via hole defined by side surfaces of the second dielectric layer and a bottom on at least a portion of the upper surface of the lower metal feature;

forming a sixth barrier layer, comprising a sixth dielectric barrier material different from the first, fourth and fifth dielectric materials, on the fifth barrier layer

overlying the third dielectric layer, on the side surfaces of the third dielectric layer defining the trench, on the side surfaces of the second dielectric layer defining the via hole, on a portion of the fourth barrier layer between the trench and via hole, and at a bottom of the via hole;

etching to remove the sixth barrier layer from, and stopping on, the fifth barrier layer, from and stopping on the fourth barrier layer, and at the bottom of the via hole, leaving a portion of the sixth barrier layer as a liner on the side surfaces of the third dielectric layer defining the trench and on the side surfaces of the second dielectric layer defining the via hole; and

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filling the dual damascene opening with metal to form a metal line connected to an underlying metal via.

7. (Original) The method according to claim 6, comprising filling the dual damascene opening with copper (Cu) or a Cu alloy to form a Cu or Cu alloy line connected to a Cu or Cu via which is electrically connected to the lower metal feature.

8. (Original) The method according to claim 7, wherein the lower metal feature comprises a Cu or Cu alloy line.

9. (Original) The method according to claim 7, wherein the dual damascene opening is misaligned with respect to the lower metal feature such that the bottom of the via hole is on a portion of the upper surface of the lower metal feature and on a portion of an upper surface of the first barrier layer.

10. (Original) The method according to claim 6, further comprising depositing a seventh barrier layer, comprising a seventh dielectric barrier material, on an upper surface of the sixth barrier layer and on an upper surface of the metal line.

11. (Original) The method according to claim 6, wherein the first, second, third, fourth, fifth and sixth dielectric barrier materials are selected from the group consisting of silicon nitride, silicon carbide and silicon oxynitride.

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12. (Original) The method according to claim 6, comprising depositing each of the first, second, third, fourth, fifth and sixth barrier layers at a thickness of about 50Å to about 500Å.

Claims 13 through 20. (Withdrawn)

21. (Currently amended) The method according to claim 1, comprising etching to form the ~~first~~ single opening having entire side surfaces which are substantially parallel.